Amendments to the Claims:

1. (Currently Amended) A method for performing technology mapping, the method comprising:

a) receiving ~~a~~ an IC design layout that is not bounded to a particular technology;

b) repeatedly:

selecting from the IC design layout a candidate sub-network;

identifying at least one replacement sub-network from a storage structure that stores replacement sub-networks that are bound to the particular technology; and

replacing the selected candidate sub-network in the IC design layout with the replacement sub-network;

~~c)~~ wherein at least a particular one of the selected candidate sub-networks has multiple circuit elements that provide ~~multiple outputs~~ at least three output Boolean functions of the particular candidate sub-network.

2. (Original) The method of claim 1, wherein identifying the replacement sub-network comprises:

generating a parameter based on a set of output functions performed by the selected candidate sub-network, wherein the parameter identifies the replacement sub-network.

3. (Original) The method of claim 2 further comprising: using the parameter to retrieve the replacement sub-network from the storage structure.

4. (Canceled)

5. (Canceled)

6. (Original) The method of claim 1 further comprising:

terminating the repetitions once a stopping criteria is reached.

7. (Currently Amended) The method of claim 6, wherein the IC design layout includes a plurality of circuit elements and the sub-networks are formed by circuit elements, the method further comprising:

after terminating the repetitions, traversing the IC design layout to identify circuit elements that are not bound to the technology;

for each identified circuit element, attempting to identify a replacement sub-network that is stored in the storage structure; and

if at least one replacement sub-network for an identified circuit element is identified, replacing the circuit element in the IC design layout with the identified replacement sub-network.

8. (Original) The method of claim 7, wherein if more than one replacement sub-networks are identified for a circuit element, selecting one of the replacement sub-networks and replacing the circuit element with the selected replacement sub-network.

9. (Canceled)

10. (Original) The method of claim 7, wherein each circuit element performs a function, wherein if no replacement sub-network is identified for an identified circuit element, decomposing the function of the circuit element into a set of functions, and then attempting to identify a set of replacement sub-networks in the storage structure that perform the set of functions.

11. (Canceled)

12. (Canceled)

13. (Original) The method of claim 1 further comprising:

before replacing the candidate sub-networks with the replacement sub-networks, evaluating whether to replace the selected candidate sub-network with the replacement sub-network,

wherein certain candidate sub-networks are replaced by replacement sub-networks based on the evaluation,

wherein certain candidate sub-networks are not replaced based on the evaluations.

14. (Original) The method of claim 13, wherein the evaluating comprises computing a cost function.

15. (Currently Amended) A computer program embedded on a computer readable medium, the computer program for receiving a an IC design layout that is not bounded to a particular technology and for mapping the IC design layout to the particular technology, the computer program comprising:

a first set of instructions for selecting from the IC design layout a candidate sub-network[[,]] ;

a second set of instructions for generating a parameter based on a set of output functions performed by the selected candidate sub-network[[,]] ;

a third set of instructions for identifying, based on the parameter, at least one replacement sub-network from a storage structure that stores replacement sub-networks that are bound to the particular technology[[,]] ;

a fourth set of instructions for replacing the selected candidate sub-network in the IC design layout with the replacement sub-network[[,]] ; and

a fifth set of instructions for repeatedly executing the first to fourth sets of instructions,

wherein at least a particular one of the selected candidate sub-networks has multiple circuit elements that provide ~~multiple outputs~~ at least three output Boolean functions of the particular candidate sub-network.

16. (Original) The computer program of claim 15, wherein the fifth set of instructions determines whether the computer program has reached a criterion for stopping the repetitions, wherein when the fifth set of instructions terminates the repetitions once the stopping criterion is reached.

17. (Currently Amended) The computer program of claim 16, wherein the IC design layout includes a plurality of circuit elements and the sub-networks are formed by circuit elements, the computer program further comprising:

a sixth set of instructions for traversing the IC design layout, after terminating the repetitions, to identify circuit elements that are not bound to the technology,

a seventh set of instructions for attempting to identify, for each identified circuit element, a replacement sub-network that is stored in the storage structure, and

an eighth set of instructions for replacing a circuit element when at least one replacement sub-network is identified for the circuit element.

18. (Previously Presented) The computer program of claim 17, wherein each circuit element performs a function, the computer program further comprising:

a ninth set of instructions for decomposing the function of a circuit element into a set of functions when no replacement sub-network is identified for a circuit element; and

a tenth set of instructions for attempting to identify a set of replacement sub-networks in the storage structure that perform the set of functions.